REMARKS

Claims 1, 2, 4-8, 11-20, and 22-26 are pending as of the Office Action mailed September 17, 2009. Claims 1, 2, 4-8, 11-20, and 22-26 stand rejected under a proposed combination of Girson et al. (U.S. Patent No. 7,111,179) and Callahan, II et al. (U.S. Patent No. 6,230,313). Claims 5 and 18 further stand rejected under a proposed combination of Girson et al., Callahan, II et al., and Choi et al. (U.S. Patent No. 6,233,690). Claims 3, 9, 10, and 21 were previously canceled. Claims 1, 13, and 22 are amended by this amendment in order to clarify certain aspects of Applicant's invention and to correct typographical errors. Support for these amendments may be found at least in paragraphs 23, 28, and 29 of the present disclosure. No new matter has been added.

In light of the following remarks, Applicant respectfully asserts that the relied upon art does not teach or suggest the recited subject matter of the claims as presently amended. Reconsideration of the rejection in light of the same is therefore respectfully requested.

As to claim 1, Applicant notes that this claim is now amended to recite:

> An article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to:
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> obtain from a performance monitor runtime performance data of a thread level utilization of the machine by an application during an execution of the application on the machine, wherein the runtime performance data is indicative of a set of execution characteristics of a thread of the application, including an instructions-per-clock cycle metric and a memory references-per-clock cycle metric, wherein the runtime performance data includes instruction counts, memory references, and cycle counts obtained from a timer interrupt in the performance monitor; and
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> based on the instructions-per-clock cycle metric and the memory references-per-clock cycle metric, reduce power dissipation of the machine by adjusting an operating voltage or an operating frequency of the machine during the execution of the application, wherein the operating voltage and operating frequency are nonzero.

Applicant respectfully submits that Girson et al. and Callahan, II et al., whether taken alone or in combination, fail to teach or suggest, among other things, "based on the instructions-per-clock cycle metric and the memory references-per-clock cycle metric,

reduc[ing] power dissipation of the machine by adjusting an operating voltage or an operating frequency of the machine during the execution of the application."

More specifically, Applicant notes that Callahan, II et al. is directed to a system for generating execution trace information related to performance measures during execution of a task. Col. 7, l. 20-28. A task, as that term is used in Callahan, II et al., is a user program. Col. 2, l. 18-21. By adding instructions to source code of the task and executing the added instructions, the execution trace information is generated. Col. 8, l. 19-25. The execution trace information is then written in hexadecimal form to an execution trace information file. Col. 16, l. 66 - Col. 17, l. 6. After the execution trace information file is generated, a description file is used to assign meaning to the information in the execution trace information file, and additional operations are then performed in order to make the execution trace information more useful. Col. 17, l. 47-51. Appropriate trace information is then extracted from the execution trace information file for display to a user. Col. 23, l. 12-15.

The Office Action relies on Callahan, II et al. as teaching, through the disclosure of the execution trace information, monitoring of thread level runtime performance data which includes a memory references-per-clock cycle metric. The Office Action states that it would have been obvious to a person of ordinary skill in the art to "employ the memory references-per-cycle metric as taught by Callahan." Office Action, page 3. The Office Action further asserts that one of ordinary skill in the art would have been motivated to do so "that power *can be saved.*" Office Action, page 3. For multiple reasons, each of which is discussed in detail below, Applicant strongly disagrees.

As noted above, Callahan, II et al. discloses that the execution trace information, which the Office Action cites as including the claimed memory references-per-clock cycle metric, is generated by executing instructions that are **added** to source code of the task (i.e., the program whose performance is to be measured). Callahan, II et al. does not disclose that the execution trace information can be generated without adding such instructions. Accordingly, "employing" the cited memory references-per-clock cycle metric of Callahan, II et al. would involve adding instructions to a program to measure the rate of memory references, thereby increasing the total number of instructions to be executed and

thereby increasing the load on the processor. This increase of the processor load would result in an *increase* in the power dissipation of the machine because, as noted in the present disclosure at paragraph 23, the number of instructions executed by a program affects the amount of power dissipated. Because "employing" the teachings of Callahan, II et al. would result in an increase in power dissipation, Applicant respectfully submits that Girson et al. and Callahan, II et al. would not be combined in order to meet the requirement of claim 1 of "based on the instructions-per-clock cycle metric and the memory references-per-clock cycle metric, *reduc[ing] power dissipation of the machine* by adjusting an operating voltage or an operating frequency of the machine during the execution of the application."

Moreover, with reference to Girson et al., Applicant notes that column 2, lines 46-53 of Girson et al. explain that this reference is generally directed to reducing the power consumption of electronic devices, and that such a reduction may be based in part on a number of instructions-per-cycle. As noted in M.P.E.P. section 2143.01.V, however, if a proposed combination of a primary prior art reference with another prior art reference would change the principle of operation of the primary reference, "then the teachings of the references are not sufficient to render the claim[ ] *prima facie* obvious." In the present case, the Office Action proposes combining Girson et al. with Callahan, II et al., which requires adding instructions to generate execution trace information, as discussed above. In light of the remarks above, such a combination would not result in the claimed invention. Instead, Applicant respectfully submits that such a combination would change the principle of operation of Girson et al. by negating Girson et al.'s objective of reducing power consumption based on instructions-per-cycle. Thus, under M.P.E.P. section 2143.01.VI, the proposed combination of Girson et al. and Callahan, II et al. is insufficient to establish obviousness of amended claim 1.

For each of the above reasons alone, Applicant respectfully submits that claim 1 is in condition for allowance.

To expedite the prosecution of this application, however, Applicant further notes that the aforementioned limitation of amended claim 1 requires "based on the instructions-per-clock cycle metric *and the memory references-per-clock cycle metric*, reduc[ing] power dissipation of the machine by adjusting an operating voltage or an operating

frequency of the machine *during the execution of the application*." As noted above in the discussion of Callahan, II et al., the execution trace information is generated during execution of a user program. However, as discussed in detail below, in Callahan, II et al., the execution trace information cannot be utilized until **after** the execution of the user program has completed. Consequently, it is submitted that the combination of Callahan, II et al. and Girson et al. does not teach or suggest the aforementioned limitation of amended claim 1.

More specifically, Callahan, II et al. discloses in column 6, lines 62-66 that the execution trace information file is "examined" **after** execution of the task, i.e., the user program, has completed. Additionally, as best understood from Callahan, II et al., "examining" the execution trace information file involves, at the very least, assigning meaning to the information in the file using the description file as discussed above. Accordingly, the execution trace information is not assigned meaning, and therefore cannot be utilized, until **after** the execution of the user program has completed. Thus, even if the Examiner considers the execution trace information to include the claimed memory references-per-clock cycle metric, and even if the Examiner considers the user program of Callahan, II et al. to be equivalent to the application recited in amended claim 1, positions which the Applicant does not take, the combination of Callahan, II et al. and Girson et al. nonetheless fails to teach or suggest the aforementioned limitation of amended claim 1. If the Examiner is of a differing opinion as to when the "examining" step of Callahan, II et al. occurs or as to what this "examining" step involves, Applicant respectfully requests a showing with particularity as to a contrary teaching by Callahan, II et al. Absent such a showing, it is respectfully submitted that claim 1 is in condition for allowance for these additional reasons as well.

Claims 13 and 22 have also been amended to include limitations that are the same as or similar to limitations discussed above with respect to claim 1. Consequently, Applicant respectfully submits that the proposed combination of Girson et al. and Callahan, II et al. fails to render obvious claims 13 and 22 for reasons similar to those discussed above. Claims 13 and 22 are therefore in condition for allowance.

As to claims 2, 4-8, 11, 12, 14-20, and 23-26, each of these claims depends from either claim 1 (claims 2, 4-8, 11, and 12), claim 13 (claims 14-20), or claim 22 (claims

23-26). Accordingly, Applicant respectfully submits that each of claims 2, 4-8, 11, 12, 14-20, and 23-26 are patentable and in condition for allowance for at least the same reasons as their respective independent claims.

Claims 5 and 18 further stand rejected under a proposed combination of Girson et al., Callahan, II et al., and Choi et al. Claim 5 depends from independent claim 1, and claim 18 depends from independent claim 13. In light of the relevant remarks above as to the failure of the combination of Girson et al. and Callahan, II et al. to render independent claims 1 and 13 obvious, Applicant respectfully submits that claims 5 and 18 are patentable and in condition for allowance for at least the same reasons as their respective independent claims.

CONCLUSION

In light of the foregoing, applicant respectfully asserts that claims 1, 2, 4-8, 11-20, and 22-26 are in condition for immediate allowance. A prompt indication of allowability is earnestly solicited.

Should the examiner wish to discuss the foregoing, or any matter of form in an effort to advance this application toward allowance, he is urged to telephone the undersigned at the indicated number.

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Respectfully submitted,

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